

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Kimihiro MAEMURA

Application No.: New U.S. Patent Application

Filed: February 23, 2004

Docket No.: 118806

For: NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE

INFORMATION DISCLOSURE STATEMENT


Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

- ☒ 1. This Information Disclosure Statement is being filed (a) within three months of the U.S. filing date of this non-CPA application, OR (b) before the mailing date of a first Office Action on the merits in the present application. No certification or fee is required.
- ☒ 2. Relevance of the non-English language references 8-9 is discussed in the present specification.
- ☒ 3. The present application was filed or entered the U.S. National Stage of the PCT after June 30, 2003. In accordance with the June 11, 2003, Notice waiving the requirements of 37 C.F.R. §1.98(a)(2)(i), copies of any U.S. patents and patent application publications are not attached.
- ☒ 4. English-language Abstracts of the non-English language references 4, and 7-9 are attached hereto.
- ☒ 5. Reference 9 corresponds to reference 4, therefore a translation is not attached.

Respectfully submitted,



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Form PTO-1449 (REV. 8-83)		US Dept. of Commerce PATENT & TRADEMARK OFFICE		ATTY DOCKET NO. 118806		APPLICATION NO. New U.S. Application	
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)				APPLICANT Kimihiro MAEMURA			
				FILING DATE February 23, 2004			
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	
	1	US 6,255,166 B1	07/03/2001	OGURA et al.			
	2	US 6,248,633 B1	06/19/2001	OGURA et al.			
	3	US 6,177,318 B1	01/23/2001	OGURA et al.			
	4	5,969,383	10/19/1999	CHANG et al.			
	5	5,494,838	02/27/1996	CHANG et al.			
	6	5,422,504	06/06/1995	CHANG et al.			
	7	5,408,115	04/18/1995	CHANG			
FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	
	8	JP A 6-181319 w/ abst & trans	06/28/1994	Japan			
	9	JP A 11-074389 w/ abst	03/16/1999	Japan			
	10	JP B1 2978477 w/ trans	09/10/1999	Japan			
	11	JP A 2001-156188 w/ trans	06/08/2001	Japan			
	12	JP A 7-161851 w/ trans	06/23/1995	Japan			
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)							
	13	Hayashi, Yutaka et al. "Twin MONOS Cell with Dual Control Gates." 2000 Symposium on VLSI Technology Digest of Technical Papers, 2000 IEEE					
	14	Chang, Kuo-Tung et al. "A New SONOS Memory Using Source-Side Injection for Programming." IEEE Electron Device Letters, Vol. 19 No. 7 (pp. 253-254) July 1998					
	15	Chen, Wei-Ming et al. "A Novel Flash Memory Device with SPlit Gate Source Side Injection and ONO Charge Storage Stack (SPIN)." 1997 Symposium on VLSI Technology Digest of Technical Papers (pp. 63-64)					
EXAMINER					DATE CONSIDERED		
Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

Date: February 23, 2004